PATENT
1110-0289P

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Hiroshi MURAKAMI

Rule 53(b) Divisional
Application of Application No.: 08/873,463

Filed: May 7, 2001

For: IMAGE FILTER CIRCUIT

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

May 7, 2001

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE ABSTRACT

Please replace the original Abstract page with the replacement Abstract page attached hereto.

IN THE SPECIFICATION

Page 2

Line 1, delete ", and thus," and insert --. Thus,--;

Line 8, delete "an" and insert --a--;

Line 16, after "and" insert --is--.

Page 3

Line 2, after "and" insert --are--.

Page 4

Line 10, after "or" insert --the--.

Page 20

Line 23, after "of" insert --the fact--.

Page 29

Line 4, after "invention" insert --preferably--;

Line 6, delete "as well" and insert --. It further preferably--;

Line 7, delete "as" first occurrence.

IN THE CLAIMS

Please cancel original claims 1-5 without prejudice or disclaimer to the subject matter contained therein.

Please add the following new claims:

-- 6. An image processing device for carrying out a dodging treatment, comprising:

a luminance image signal generator for generating a luminance image signal from input color image signals;

a filter for filtering said luminance image signal to generate an unsharp image signal;

a dynamic range compressor for subjecting said unsharp image signal to a dynamic range compression treatment to generate a compressed unsharp image signal for the dodging treatment;

at least one memory for delaying said input color image signals for a time period corresponding to a delay time during which said compressed unsharp image signal for the dodging treatment is generated from said input color image signals;

an adder for subtracting said compressed unsharp image signal for the dodging treatment from each of delayed input color image signals.

7. The device according to claim 6, wherein said filter is an IIR type filter.

8. The device according to claim 6, wherein said at least one memory comprises a plurality of FIFO type field memories disposed in parallel, and image signals are written to one FIFO type field memory and read-out from one other FIFO type field memory, sequentially.

9. The device according to claim 6, further comprising, a main controller for generating signals which control writing to and reading from said at least one memory to control the operation time of said at least one memory in accordance with the delay time of said image signals at said filter.

10. The device according to claim 9, wherein said main controller includes a first counter which counts a number of pixels in horizontal and vertical directions of a reproduced image; a first flip-flop which generates said signals controlling writing during a time period from when said first counter starts counting until the end of counting; a

second counter which starts counting a number of horizontal and vertical delays of said image signals at said filter, beginning when said first counter starts counting; a third counter which starts counting the number of horizontal and vertical delays of said image signals at said filter, after said first counter has finished counting; and a second flip-flop which generates said signals controlling reading after said second counter has finished counting, and until a time period when said third counter finishes counting.

11. The device according to claim 7, wherein said IIR type filter is at least one of a low-pass filter and an all-pass filter.

12. The device according to claim 6, wherein said luminance image signal generator is a matrix calculator.

13. The device according to claim 6, wherein said dynamic range compressor subjects to said dynamic range compression treatment using a dynamic range compression table. --

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 6-13 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Donald J. Daley, Reg. No. 34,313 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: ______________________
Donald J. Daley, Reg. No. 34,313

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

DJD/MJL:kna

ABSTRACT OF THE DISCLOSURE

An image filter circuit generates unsharp image signals to subject image signals to a dodging treatment which adjusts areas of exposure over an entire image within an image processing apparatus for image processing the image signals. The circuit includes an IIR type filter for carrying out a filtering treatment to generate the unsharp image signals. It further includes a FIFO type field memory for delaying image signals which are not subjected to the filtering treatment at the IIR filter for a time corresponding to the delay time of image signals which have been subjected to the filtering treatment at the IIR type filter. The image filter circuit, which obtains the unsharp image signals corresponding to an unsharp mask for obtaining a dodging effect, can be made small in size with a simplified circuit arrangement.